# RC NETLIST REDUCTION FOR TIMING AND NOISE ANALYSIS

## Abstract

A circuit reduction method that generates a netlist that maintains a topology of an original circuit while preserving an original circuit's functions and characteristics is provided. Further, a circuit reduction method that allows a user to selectively determine which nodes of an original circuit to reduce is provided. Further, a circuit reduction tool that is capable of removing loops that are not present in an original circuit but are present in an extraction of the original circuit is provided.

18572_1